REMARKS

Applicants respectfully request reconsideration of this application as amended. Claims 1, 2, 10, 18, 20, 23, and 24 have been amended. No claims have been canceled. Therefore, claims 1-29 are now presented for examination.

In the advisory action mailed 4/22/2004 the Examiner withdrew the rejection of claims 1-29 under 35 U.S.C. §112, second paragraph, Claim 1, 18, and 24 remain rejected under 35 U.S.C. §103(a) as being unpatentable over Dangelo (U.S. Patent No.6,324,678) in view of Tabak. Applicants submit that the present claims are patentable over Dangelo in view of Tabak.

Dangelo discloses an electronic CAD system operated with a suite of software tools for enabling a designer to create and validate a structural description and physical implementation of a device from a behavior-oriented description using a high-level computer language.

The Examiner has admitted that Dangelo does not disclose an addressing matching function, lane matching function and one or more bus connections for the memory-mapped device based upon the logic design component and the first starting address. See Final Office Action mailed 4/22/2004 at page 6, paragraphs 39 and 40, and page 7, paragraphs 42-44.

Tabak discloses various microprocessor architectures. At pages 4-5 Tabak discloses a microprocessor with a large internal data bus, e.g., 32 bits and a smaller external data bus, e.g., 16-bits. At page 21 Tabak discloses several byte sizes, e,g., byte, halfword, and word, that may be sent on the data bus via a MOVB, MOVH and MOVW instruction, where for example, "MOVB src, dst" moves a byte from a source (src) address to a destination (dst) address. Tabak (pp. 48-49) further discloses address mapping, which is the mapping between main memory and a cache. The mapping operates in a manner such that, line 0 from main memory is stored in set 0 in the cache, line 1 in set 1 and so forth until the number of sets in the cache are exhausted. Then the count starts again with set 0.

Claim 1 discloses among other features: using a logic design component to specify addressability for a memory-mapped device, addressability comprising an address matching function configured to process an address range for a set of transactions at different data byte sizes, a lane matching function selecting an address in part of the address range, and one or more bus connections. This feature is supported by p. 12 of the specification, where in a 32-bit system bus, there are four different transactions that pass the address matching function for addresses 0x00000004 and 0x00000005: 1. a word-wide transaction at 0x00000004, 2. a halfword wide transaction at 0x00000004, 3. a byte wide transaction at 0x00000004, and 4. a byte wide transaction at 0x00000005. Transactions 1,2 and 3 match a first lane matching function (address 0x00000004) and transactions 1, 2, and 4 match a second lane matching function (address 0x00000005).

Tabak at p. 49 explains that the address mapping discussed is set associative and that in Fig. 4.5 at p. 50, the mapping is byte to byte not different byte sizes. While Tabak at p. 21 discloses several different byte sizes for use in a MOV instruction, each byte size is handled separately, e.g., MOVB, MOVH and MOVW, and Tabak does not disclose nor suggest an address matching function configured to process an address range for a set of transactions at different data byte sizes.

In addition Tabak at pp. 4-5 and the Examiner's arguments at para. 40 and 42 of the final office action mailed 04/22/2004 explain a form of serial to parallel conversion, e.g., 2 sequential 8-bit groups of data from an 8 bit bus onto a parallel 16-bit bus. Here, Tabak does not discuss addressing. Thus Tabak does not disclose nor suggest an address matching function configured to process an address range for a set of transactions at different data byte sizes and a lane matching function selecting an address in part of the address range.

For the above reasons alone claim 1 should be allowable.

Claims 2-9 depend from claim 1 and include additional features. Thus, claims 2-9 are also patentable over Dangelo in

view of Tabak.

Claims 18 and 24 should also be allowable for at least the same reasons claim 1 is allowable. Since claims 19-23 depend from claim 18 and include additional features, claims 19-23 are also patentable over Dangelo in view of Tabak. Since claims 25-29 depend from claim 24 and include additional features, claims 25-29 are also patentable over Dangelo in view of Tabak.

Previous claim 10 remains rejected under 35 U.S.C. §103(a) as being unpatentable for the same reasons claim 1 was rejected (para. 60 of the Final Office Action). Hence, presently amended claim 10 should be allowable for at least the same reasons claim 1 is allowable. Since claims 11-17 depend from claim 10 and include additional features, claims 11-17 are also allowable.

Claims 2-17, 19-23, and 25-29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Dangelo (U.S. Patent No.6,324,678) in view of Tabak and Applicants' Admission and MPEP 2144.04 (Routine Expedient of making automatic). Applicants submit that the present claims are patentable over Dangelo and Tabak even in view of background of the application.

Applicants' background discloses specifying the addressability and bus connections, and the tediousness of a designer to explicitly specify designing for 8-bit and 32-bit system busses. See Specification at pages 1 and 2. However, if anything, applicants' background teaches away from the claims since the claims recite generating first logic components that implement an address matching function, and generating second logic components that implement lane matching function and one or more bus connections.

As described above, neither Dangelo nor Tabak disclose or suggest replacing a logic design component with logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for the memory-mapped device based upon the logic design component and the first starting address. Therefore, the present claims are patentable over any combination of Dangelo, Tabak and applicants' background since none of the above disclose or

suggest replacing a logic design component with logic components that implement a first set of addressing matching function, lane matching function and one or more bus connections for the memory-mapped device based upon the logic design component and the first starting address.

Applicants respectfully submit that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on August 17, 2004.

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